Multi-Resolution Feedback to Minimize Communication Data and Improve Output Accuracy

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***Abstract* -- In this paper, a multi-resolution feedback method is proposed to reduce the communication data in isolated digital power supplies in an attempt to avoid technical and cost disadvantages of high-speed circuits. It uses only 4 bits per sample to provide 10-bit output accuracy, which is higher than existing isolated digital designs. Simulation and preliminary experimental results demonstrate the effectiveness of the proposed method.**

***Index Terms*-- communication, DC-DC power conversion, Isolated power supply, Digital control.**

I. INTRODUCTION

As the embedded computing technology becomes mature and the cost drops in accordance with Moore's law, digitally controlled power supplies are becoming a significant market opportunity [1][2]. For non-isolated power supplies, many advanced digital control methods were developed [3][4][5][6]. The controller samples the feedback signals and directly uses the data for control-law calculation; therefore data communication across the isolation boundary was never an issue.

However, an isolated digital power supply transmits a considerable amount of data from the secondary to the primary side to operate the feedback loop. The data rate is in direct proportion to the switching frequency and the ADC resolution. As is pursued by both academia and industry, higher switching frequency is desired to reduce the volume and cost of magnetic components. Higher resolution ADC is also desired as it improves the output accuracy. Therefore, the data rate in isolated digital power supplies will inevitably multiply as the technology evolves. This increasing demand for data rate brings two problems: high-speed circuits are more vulnerable in noisy environment such as power supplies, which may cause fatal failure; and high-speed circuits also dissipate more energy, which lowers the power supply efficiency. Although ultra high-speed isolators are being developed [7][8][9], they are tens or hundreds of times more expensive than commonly used logic isolators, which may prevent isolated digital power supplies from practical use. Therefore, it is important to reduce the data transfer rate without degrading the output performance.

Existing communication methods in isolated digital power supplies can be summarized into two types: transmitting duty cycle and transmitting sample data. They compromise the output performance due to the speed limits of the isolators.

In [10], a 400 KHz isolated digital power supply is designed using a secondary controller. The duty cycles are transmitted to the primary side via a 150 MHz isolator [11]. Although the digital isolator used is almost the fastest one in the market, the duty-cycle resolution is only $400\text{KHz}/150\text{MHz} \times 100\% = 0.267\%$. As a result, the ADC resolution is limited to 6-bit, otherwise limit cycle oscillation will occur [12].

In [13], high-speed isolators are used for transmitting sample data. Due to the speed limit and the inefficient protocol, only 4 LSB of an 8-bit ADC can be transmitted. Higher resolution ADCs cannot be used to improve the output accuracy because 4 LSB are too few to present the output voltage range, or the dynamic response must be compromised.

In [14], both transmitting duty cycle and transmitting sample data methods are employed. As is discussed above, the isolator's speed limit restricts the ADC resolution and as a result, only 8 MSB of a 10-bit ADC are transmitted, otherwise limit cycle oscillation will occur.

In this paper a multi-resolution feedback (MRF) method is presented which: 1) Transmits 4 bits per sample, 2) Achieves 10-bit ADC resolution at the output voltage level, 3) Lowers the ADC resolution requirement when the output voltage deviates from the reference voltage level, thus covering ±5% output voltage range, which is sufficient for most applications.

The proposed method significantly reduces the data rate in isolated digital power supplies and thereby: 1) Reduces the cost for high-speed isolators, 2) Reduces design difficulties of the high-speed circuitry, 3) Reduces the energy dissipated by the high-speed circuitry. Furthermore, the output accuracy is better than existing designs.

In this paper, Section II. describes the concept of the multi-resolution feedback method, and presents design guide lines; Section III. shows its effect on dynamic response through simulation; Section IV. demonstrates the implementation and the experimental results.

II. MULTI-RESOLUTION FEEDBACK METHOD

The multi-resolution feedback (MRF) method is based on the idea that output voltage samples can be compressed into a shorter length by eliminating unnecessary information, which includes unnecessary scale range and unnecessary resolution.

The output regulation range is usually defined in the design specification. Any scale range outside of the output regulation range is unnecessary information.

The highest resolution only needs to be provided around the desired output voltage point. The further away from the rated output voltage level, the less resolution is needed, as the feedback system will bring the voltage back to the desired point. If steady state error exists, the highest resolution should be provided throughout the steady state error range, as the operation point of the system can be any point in this range.

Based on above observation, an MRF lookup table is made which divides the ADC's Full Scale Range into several levels. The levels cluster around the reference voltage point providing the smallest quantization step size, and are distributed unevenly across the output regulation range. The MRF levels next to the reference voltage are 1 LSB wide which gives the maximum output accuracy. As the voltage deviates away from the reference voltage, the MRF levels become wider and wider so as to reduce the total number of levels. All ADC samples are mapped into the MRF levels and then encoded into MRF codes that are much shorter than the original ADC sample length. The MRF codes are transmitted through the isolator with a protocol and are then decoded into the original sample length to take part in the control-law calculation. A concept map of MRF levels is shown in Fig. 1.

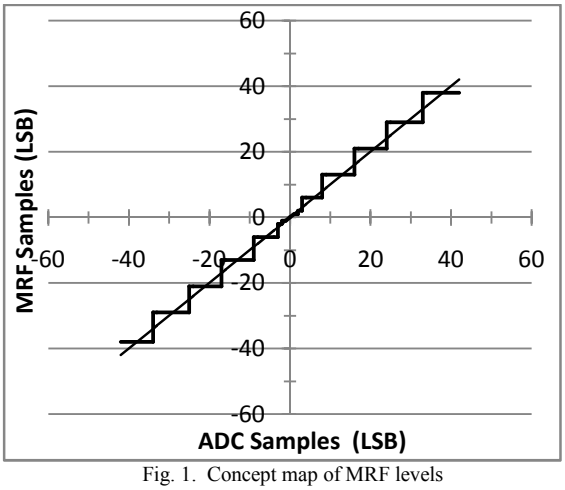


Fig. 1. Concept map of MRF levels

The effects of the MRF on transfer function can be interpreted as round-off errors in quantization effects, which can be considered as a variable gain due to the finite resolution in the realization of the analog-to-digital converter [15]. In MRF, the round-off errors are smaller around the output voltage level; and the errors are larger when further away from the output voltage level, which change the variable gain range in each level. In stochastic analysis, the round-off error is a white random process with a uniform probability density from $-\frac{q}{2}$ to $+\frac{q}{2}$, where q is the step size of the quantization [15]. In MRF, the q is not a constant for each level. [15] studied the worst-case bound and concluded that a BIBO (Bounded-Input Bounded-Output) system with round-off error is still BIBO stable.

Not only is a system BIBO stable with MRF, but also the transfer function is changed very little by the MRF. In MRF, the step size is 1 LSB at the reference voltage, which means that the variable gain introduced by MRF is 1 in steady state. Although the MRF introduces relatively large sample error where the resolutions are coarse, the worst-case gain in each level is bounded in a small range, because the MRF levels are designed in such a way that $V_{MRF}\ /V_{error}$ is controlled within a small value (1.5 in this paper), where V_{MRF} is the decoded voltage value corresponding to the MRF level, and V_{error} is defined as $(V_{ref} - V_{ADC})$. For example, at $V_{error} = 0.04V$ where the nearest MRF level is 0.05V, the equivalent extra gain is 1.25; at $V_{error} = 0.4V$ where the nearest MRF level is 0.5V, the equivalent extra gain is still 1.25, whereas the resolution at 0.4V is much coarser than which at 0.04V.The MRF will keep the system stable as long as the system is designed to be stable with the variable gain taken into account. The system open-loop transfer function can be written as:

$$\widehat{H}(s) = M(V_{error}) \cdot H(s)$$

where $H(s)$ is the original open-loop transfer function, and $M(V_{error})$ is the MRF gain, which is a function of V_{error} (refer to Fig. 3, which shows the maximum MRF gain in this paper is 1.5).

A design example of the MRF lookup table is shown in Table 1 and its code distribution in the output regulation range is in Fig. 2.The MRF variable gain is plotted in Fig. 3. It is observed that in the central area the MRF variable gain is (or is very close to) 1 providing accurate feedback. The variable gains that are adjacent to the central area are the largest in the entire regulation range, because V_{error} in this area is very small and the ratio is very sensitive to the MRF step size. Nevertheless, throughout the entire regulation range, the MRF variable gain is controlled within 1.5; therefore, the MRF method should have no influence on the system stability if the gain margin is sufficient.

Table 1 MRF Design Example

V_{error} (LSB)	MRF Code	V_{MRF} (LSB)
-42 to -34	1111	-38
-33 to -25	1110	-29
-24 to -17	1101	-21
-16 to -9	1100	-13
-8 to -4	1011	-6
-3 to -2	1010	-2
-1	1001	-1
0	1000	0
1	0111	1
2 to 3	0110	2
4 to 8	0101	6
9 to 16	0100	13
17 to 24	0011	21
25 to 33	0010	29
34 to 42	0001	38

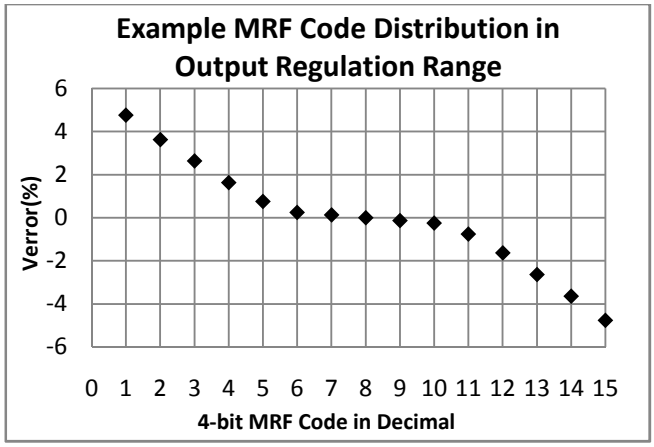


Fig. 2. Example MRF Code Distribution

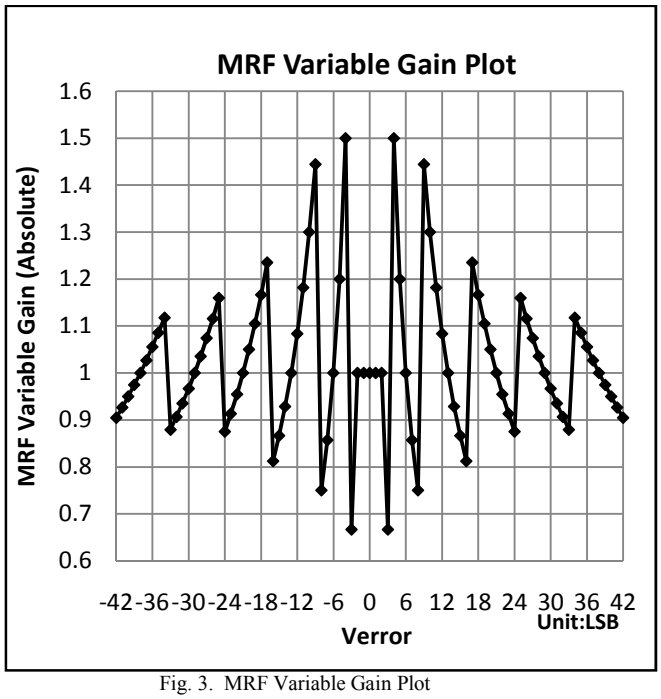


Fig. 3. MRF Variable Gain Plot

In unexpected cases where the output voltage exceeds the voltage range that the MRF levels can represent, Level 15 is always used for over voltage, and Level 0 is always used for under voltage. During the soft start, the duty cycle slowly increases regardless the feedback voltage level; the control law will not come into effect until the output voltage reaches the target level.

Three guidelines must be followed while designing a MRF system.

(1) A pole must be placed at the s-domain origin to eliminate the steady-state error. Otherwise, the output voltage may vary within the steady-state error range, and the MRF may not provide enough resolution at the operation point.

(2) Sampling must eliminate the output ripple, because the MRF only provides the highest resolution at the objective output voltage point.

The variable gains near the reference level should be suitably small to avoid changing the dynamic response of the system.use

III. Simulation Results

In order to compare the performances of the MRF-embedded and the non-MRF systems, a digital Flyback converter was simulated with and without the MRF codec. The switching frequency is 100 KHz. Vin=48±5VDC, Vo=5V/25W. The transformer turns ratio is 6:2 and the primary inductance is 15 uH.

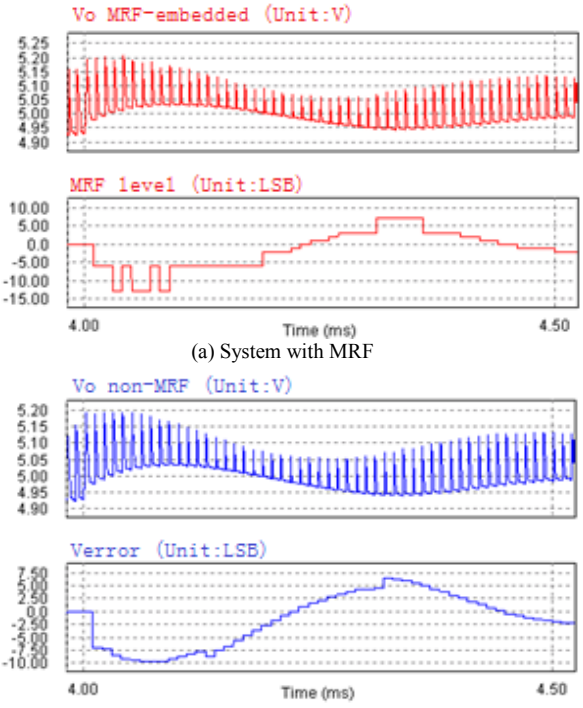
Apply the example MRF lookup table shown in Table 1 to the digital Flyback converter, where the ADC Full Scale

Range is 6.42V and 1 LSB is 6.27mV. It is discovered in design practices that when 1 LSB represents 0.12% of the output voltage, the 4-bit MRF code providing 16 MRF levels can sufficiently cover ±5% of the output voltage range; whereas 3-bit MRF only provides 8 levels which are not sufficient and 32 levels for 5-bit MRF are more than necessary.

The simulation results are shown in Fig. 4 and Fig. 5.

Fig. 4 shows the load transient response from 75% to 25% load. The two waveforms in Fig. 4 (a) are from the MRF-embedded system; the two waveforms in Fig. 4 (b) are from the system without the MRF. MRF level is the Verror signal encoded by the MRF codec. Verror is the original error signal. It can be observed that although the MRF level waveform shows obvious MRF characteristics – coarse resolution at large error values – the output voltage waveforms from the two systems are almost identical.

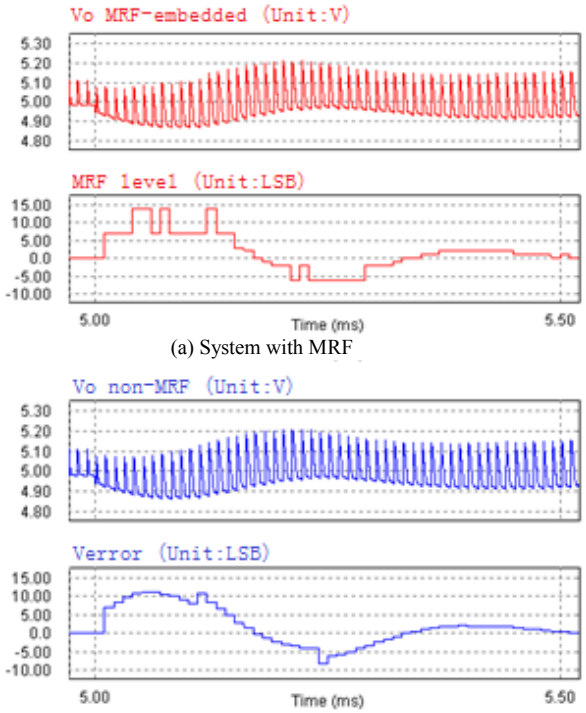
Fig. 5 shows the load transient response from 25% to 75% load. Again, a comparison of the waveforms from the two systems shows that the MRF method has no visible influence on the system's dynamic response.



(a) System with MRF

(b) System without MRF

Fig. 4. Simulation results (75% to 25% load step)



(a) System with MRF

(b) System without MRF

Fig. 5. Simulation results (25% to 75% load step)

IV. Experimental Results

A prototype of the proposed MRF method was implemented with the digital Flyback converter designed in Section III. , shown in Fig. 6. A protocol is used to transmit the MRF codes from the secondary to the primary side. Two Microchip PIC30F2020 microcontrollers are used to implement the secondary ADC/encoder and the primary decoder/compensator/DPWM, respectively. The secondary controller over-samples the output voltage in order to average out the ripple. It senses the negative pulses of the secondary winding in order to synchronize the sampling of each cycle.

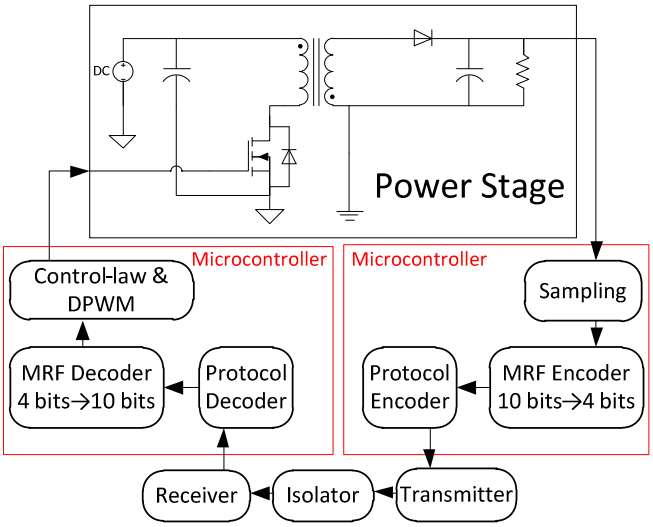


Fig. 6. Prototype Block Diagram

An electronic load in constant resistance mode is used in the test. In step load transient, the slew rate is set to 500mA/us. The experimental results are shown in Fig. 7 to Fig. 9.

During the 75% to 25% step load transient, the output voltage overshoots to 5.1V, and then undershoots to 4.95V, and returns to steady state. This waveform shows that the Verror during the load transient does not exceed the ±5% output regulation range. It proves that the MRF design covers adequate output regulation range. The waveform also shows no visible nonlinear characteristic.

During the 25% to 75% step load transient, the output voltage drops to no less than 4.85V. This waveform also proves that the MRF design covers adequate regulation range, and it shows no visible nonlinear characteristic.

Fig. 8 shows the steady state output waveforms. CH 1 is V_o. CH 3 is V_o, AC coupled. CH4 is I_o, resistive load.

Fig. 9 demonstrates the excellent output accuracy of the proposed MRF system. Throughout the output current range and the input voltage range, the output voltage is regulated within 1 LSB, 0.12%, from the rated 5V output.

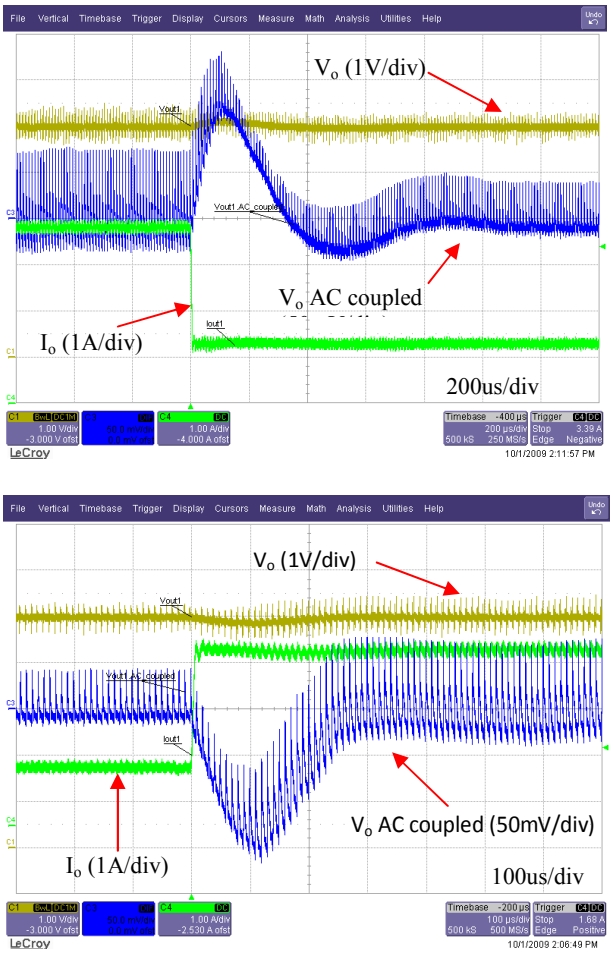


Fig. 7. Experimental results; Up: 75% to 25% load step; Down: 25% to 75% load step

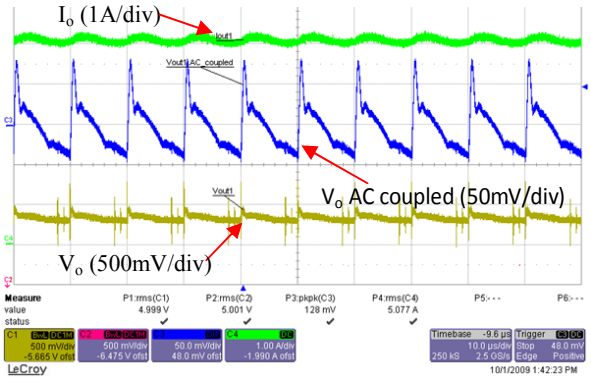


Fig. 8. Steady State Output Waveform

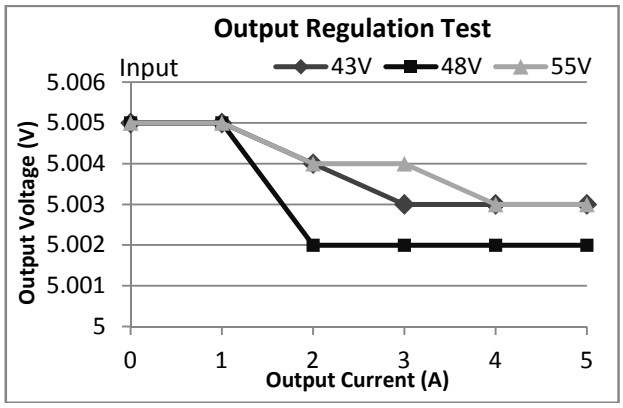
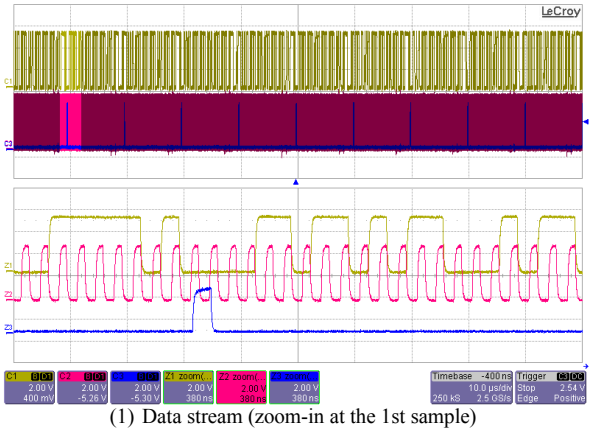


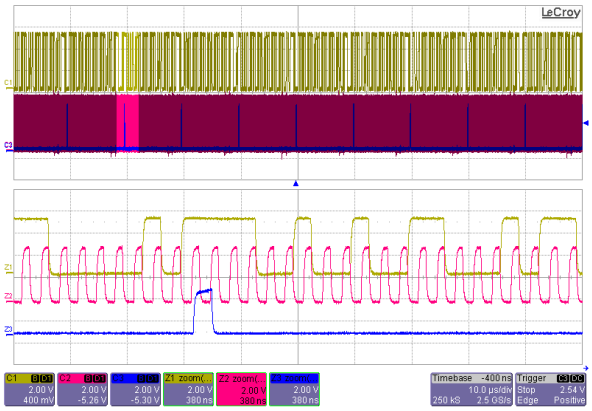
Fig. 9. Output Regulation Test

Data stream in 9 successive frames are captured in a single waveform. The waveform is then zoomed in at each frame in order to extract data that are sent from the secondary to the primary, shown in Fig. 10. This examines steady state operation, and allows us to verify precisely if the MRF has impact on the system stability.

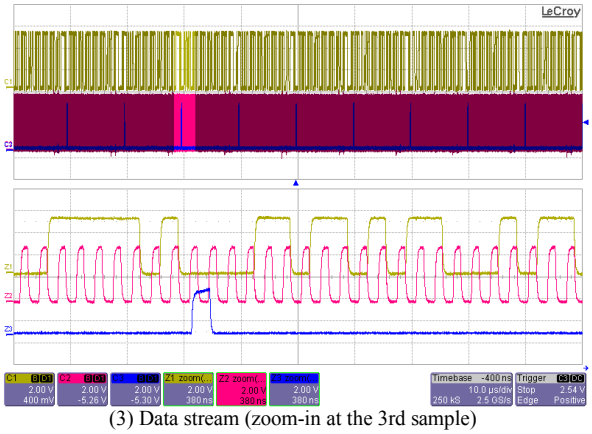
The prototype implements two independent Flyback converters on the board, and the protocol transmits two 4-bit MRF samples together for two converters; therefore the MRF method is tested by two instances in this prototype to ensure its validity.



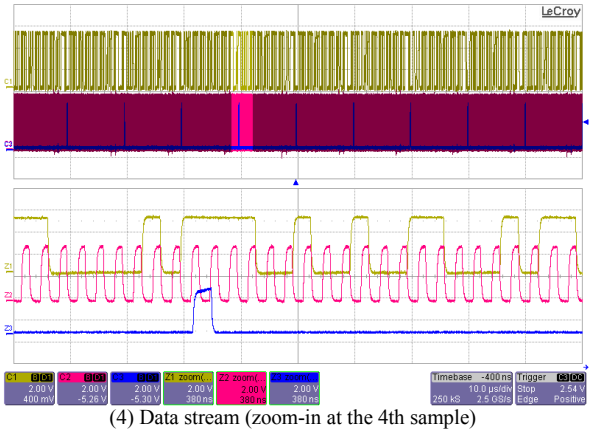
(1) Data stream (zoom-in at the 1st sample)



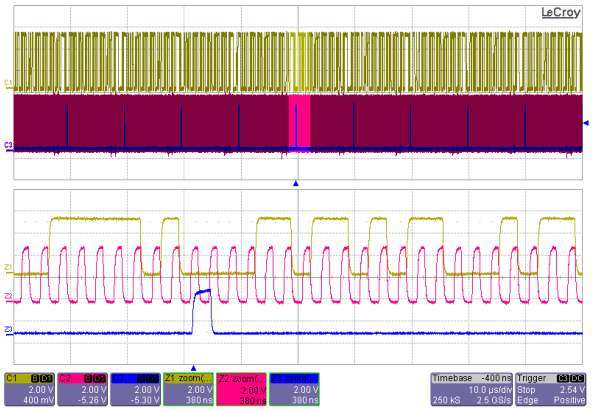
(2) Data stream (zoom-in at the 2nd sample)



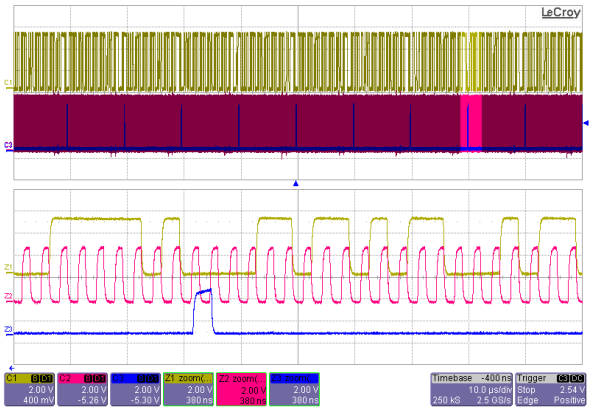
(3) Data stream (zoom-in at the 3rd sample)



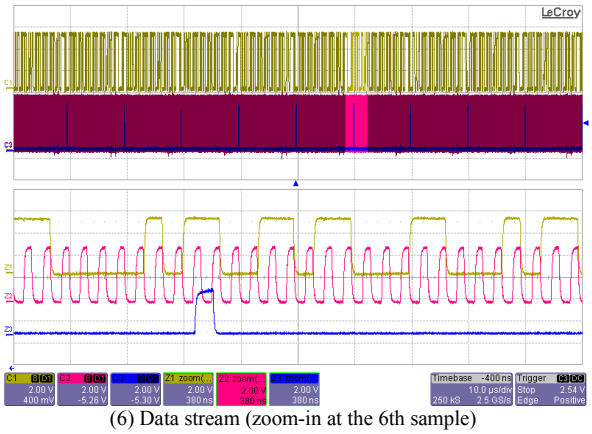
(4) Data stream (zoom-in at the 4th sample)



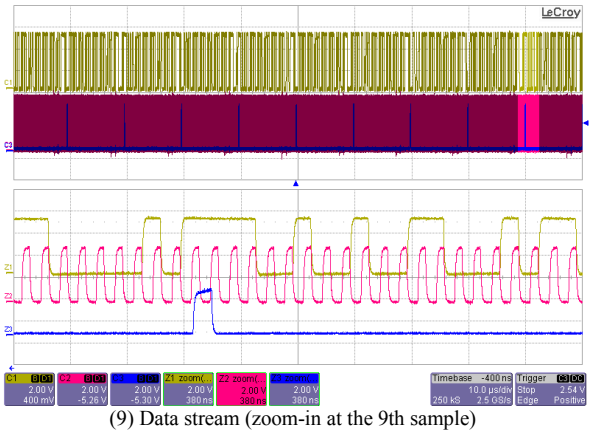
(5) Data stream (zoom-in at the 5th sample)



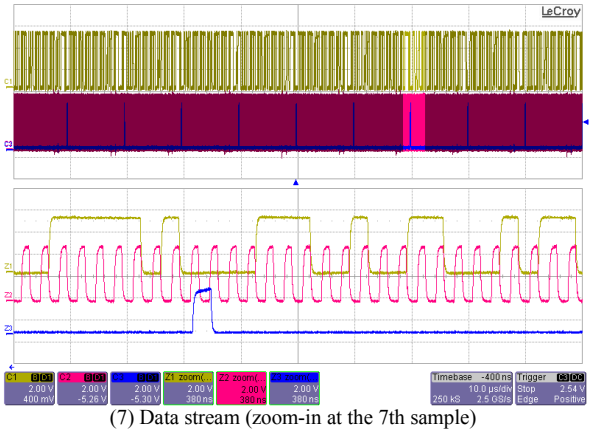
(8) Data stream (zoom-in at the 8th sample)



(6) Data stream (zoom-in at the 6th sample)



(9) Data stream (zoom-in at the 9th sample)



(7) Data stream (zoom-in at the 7th sample)

Fig. 10. Data stream in 9 successive frames. Ch1 (yellow): Data, Ch2 (red): Clock, Ch3 (blue): Frame Header.

The extracted data are given in Table 2, which shows that the output voltages are regulated within 1 LSB of the reference level (1000).

Table 2 Extracted data from 9 successive frames

Frame #	Protocol Code	MRF	
		CH1	CH2
1	0011111010	Delimiter	
	0001101101	1000	1000
2	1100000101	Delimiter	
	1110010010	1000	1000
3	0011111010	Delimiter	
	0001101101	1000	1000
4	1100000101	Delimiter	
	1110010010	1000	1000
5	0011111010	Delimiter	
	0001101101	1000	1000
6	1100000101	Delimiter	
	1001101100	0111	1001
7	0011111010	Delimiter	
	0001110010	1000	0111
8	0011111010	Delimiter	
	0001101101	1000	1000
9	1100000101	Delimiter	
	1110010010	1000	1000

V. CONCLUSION

In this paper, a Multi-Resolution Feedback method is proposed. It significantly reduces the communication data for isolated digital power supplies, thus reduces the system cost and the design difficulties. It also provides improved output accuracy than existing solutions. It uses only 4 bits per sample to achieve the accuracy that will otherwise use 10 bits to achieve. It is demonstrated through simulation and experimental results that the MRF method has no influence on system stability and no visible impact on the system's dynamic responses.

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